

A Semi-Monolithic Wideband VCO with Output Power Control Capability Using an Active Power Splitter

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ABSTRACT

One-octave bandwidth semi-monolithic VCO which has output power control capability has been developed using an active power splitter. This novel VCO exhibits an output power of 13.6 ± 1.2 dBm, output power control variation of 30 dB and output power match between two output ports is less than 0.6 dB over 8.8 to 17.6 GHz.

INTRODUCTION

Wideband oscillators are one of the key components for modern microwave systems such as measuring instruments, communication systems, electronic warfare systems and phase-locked oscillator systems. During the past several years, a number of broadband FET VCO's covering one-octave bandwidth between X- and Ku-bands have been reported [1-6]. However, conventional wideband VCO's

have been characterized by a large output power variation, a low output power and poor frequency pulling, therefore broadband buffer amplifiers have been cascaded [7-9]. To address these problems, the authors already proposed a new design approach to employ active match circuits instead of the conventional passive circuits in the design for output matching circuits [10,11]. In this paper, we report one-octave bandwidth VCO having the output power control capability and the power splitting function, which is designed by incorporating the active match circuit approach into the design of an active power splitter. In addition, a semi-monolithic process technique is used to fabricate the VCO. This semi-monolithic approach leads to the utmost performance by using newly developed discrete FET's and varactors.

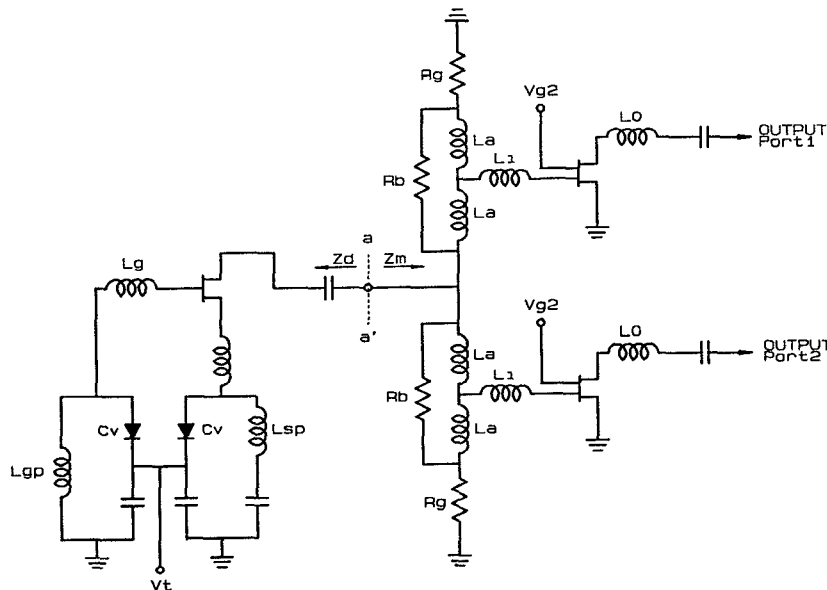


Fig.1 Schematic diagram of the VCO

CIRCUIT DESIGN

A schematic diagram of this VCO is shown in Fig.1. This circuit is divided into two circuit blocks at the reference plane a-a': the oscillator circuit block and the output matching circuit block. The outstanding feature of this design is the incorporation of an active power splitter into the design of output matching circuits. As shown in Fig.2, the input network of the active power splitter can be seen as two identical bridged-T low-impedance circuits whose input ports are linked commonly. Therefore this input network plays a role in the output matching circuit of broadband VCO's. As can be seen in Fig.3, the bridged-T low-impedance circuit is composed of six circuit elements including bridging resistor (Rb), terminating resistor (Rg), FET gate-to-source capacitance (Cgs) and three bond-wire inductances (La, Li). Furthermore, the active power splitter has the output power control capability by use of dual gate FET's.

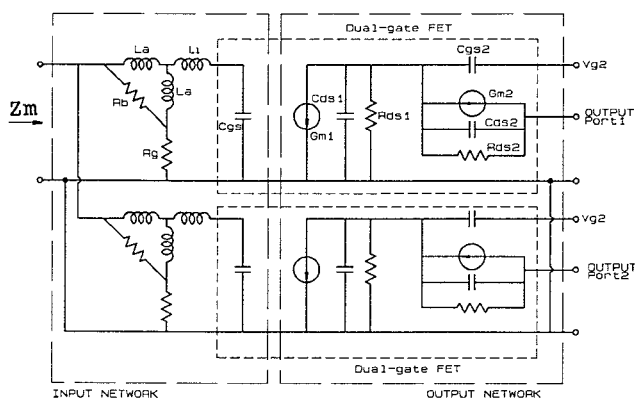


Fig.2 Equivalent circuit of the active power splitter

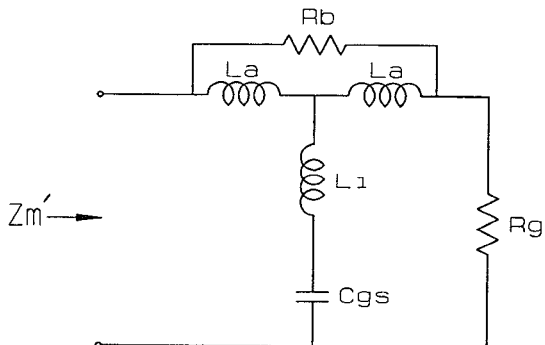
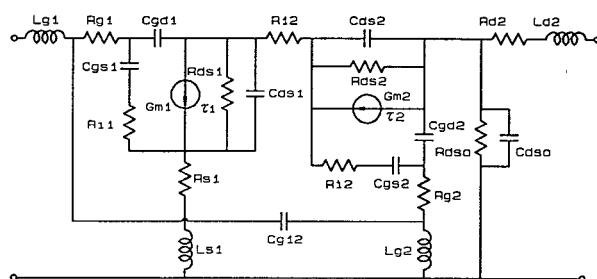


Fig.3 Equivalent circuit of the bridged-T low-impedance circuit



| | Vg2=1.2v | Vg2=0v | | Vg2=1.2v | Vg2=0v |
|------------|----------|--------|------------|----------|--------|
| Gm1 (mS) | 62 | 40 | Cgs1 (pF) | 0.24 | 0.27 |
| Gm2 (mS) | 58 | 15 | Cgs2 (pF) | 0.103 | 0.120 |
| T1 (ps) | 2.15 | 3.00 | Cgd1 (pF) | 0.010 | 0.020 |
| T2 (ps) | 4.32 | 5.10 | Cgd2 (pF) | 0.015 | 0.021 |
| Rg1 (ohm) | 1.1 | 1.0 | Cds1 (pF) | 0.064 | 0.010 |
| Rg2 (ohm) | 1.0 | 0.9 | Cds2 (pF) | 0.060 | 0.009 |
| Ri1 (ohm) | 0.83 | 1.50 | Cg12 (pF) | 0.013 | 0.008 |
| Ri2 (ohm) | 0.83 | 0.80 | Lg1 (nH) | 0.04 | 0.04 |
| Rds1 (ohm) | 100 | 40 | Lg2 (nH) | 0.02 | 0.02 |
| Rds2 (ohm) | 130 | 300 | Li (nH) | 0.03 | 0.03 |
| Rs1 (ohm) | 0.8 | 0.8 | Ld1 (nH) | 0.05 | 0.05 |
| Rd2 (ohm) | 1.3 | 1.3 | Rdso (ohm) | 4800 | 4200 |
| Rl2 (ohm) | 3.1 | 3.0 | Cds0 (pF) | 0.065 | 0.080 |

Fig.4 Equivalent circuit of the dual gate MESFET (CF007-01)

Approximately, the cutoff frequency of the bridged-T low-impedance network can be derived as:

$$f_c \approx (2Cgs(La+2Li))^{\frac{1}{2}}/\pi \quad (1)$$

The oscillator circuit was designed by using a double-tuned VCO topology shown in Fig.1. As a tuning varactor, GaAs hyperabrupt varactors (M/A-COM MA46470) were used, which have a capacitance ratio of 10:1 and a capacitance of 0.5 pF at 4 V. The Q factor is more than 4000. As an oscillator source FET and an output matching circuit FET, 0.3 X 300 micron GaAs MESFET (TOSHIBA JS8818A-AS) and 0.3 X 300 micron GaAs dual gate MESFET's (CELERITEK CF007-01) were chosen respectively, considering the operating frequency up to 18 GHz of VCO's. Fig.4 shows the equivalent circuit and element values of the dual gate FET which were derived from measured DC- and S-parameters. Using these devices, the oscillator circuit elements (Lg, Lgp, Lsp) and output matching circuit elements (Rb, Rg, La, Li) were designed to satisfy the following conditions (2) and (3) for X to Ku band.

$$\begin{aligned} \text{Re}[Z_d] &< -50 \text{ ohm} & \text{Im}[Z_d] &= 0 \text{ ohm}, & (2) \\ \text{Re}[Z_m] &= 15 \text{ ohm} & \text{Im}[Z_m] &= 0 \text{ ohm}, & (3) \end{aligned}$$

where Z_d and Z_m are an output impedance of the oscillator circuit and an input impedance of the output matching circuit respectively. The condition (2) and (3) are based on small signal designs.

FABRICATION

A photograph of the VCO appears in Fig.5. A thin film technology, so called "semi-MMIC"[12], make it possible to fabricate all passive elements including air bridges and MIM capacitors and thin film resistors on alumina substrate monolithically. The air bridges are formed by using multicoated photoresist and selective electroplating. A SiO_2 dielectric film is deposited by reactive sputtering as a dielectric layer of the MIM capacitor. The TaN film is used as a material of the thin film resistors for its good thermal stability. These passive elements are fabricated on high quality alumina substrate with a purity of 99.8 % and thickness of 0.38 mm. This substrate has four small

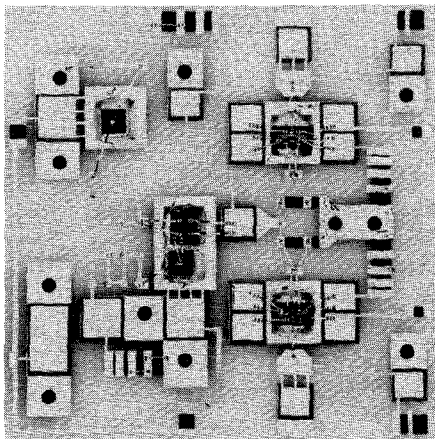


Fig.5 Photograph of the semi-monolithic VCO

hollows with a depth of 0.12 mm, where active devices are inserted not only for heat sink but also for minimizing bond-wire inductances. Frequency adjustment was achieved by tuning the inductances, L_g , L_{gp} , L_{sp} as shown in Fig.1, and these inductances are fabricated with any number of air bridges for the purpose of higher Q factor of the circuit. Two varactors are biased at the same supply voltage. The circuit size is 4.5 X 4.5 mm. A profile of the semi-MMIC circuit is shown in Fig.6.

PERFORMANCE

Measured tuning bandwidth and output power of port 1, port 2 are shown in Fig.7. It can be seen that a tuning bandwidth of 8.8 to 17.6 GHz is achieved when the tuning voltage is varied from 1.0 to 20 V. In this frequency range, output power of port 1, port 2 are 13.6 ± 1.2 dBm and 13.4 ± 1.2 dBm respectively, and power match between two output ports is less than 0.6 dB. Fig.8 and 9 display measured output power and the oscillation frequency variation as a function of the second gate voltage, respectively. Varying second gate voltage 1.2 to -1.2 V, this VCO exhibits very flat power response across the 8.8 to 17.6 GHz band and approximately 30 dB output power control variation. As shown in Fig.9, maximum frequency variation is 180 MHz when second gate voltage is varied between 1.2 to 0 V. Other measured performance of the VCO are summarized in Table 1. Maximum frequency pulling of 50 MHz into 1.7 : 1 load VSWR and phase noise of -70 dBc/Hz (100 KHz off-carrier) are also obtained for 8.8 to 17.6 GHz. The three of FETs are biased at $I_{ds} = 0.5I_{dss}$, $V_{ds} = 4.0$ V by using self-biasing configuration.

CONCLUSION

A 8.8 to 17.6 GHz broadband VCO having the output power control capability and the power splitting function has been designed and fabricated in semi-monolithic form. This semi-monolithic approach provides significant advantages throughout performance, cost, reliability, reproducibility and manufacturing cycles. This novel VCO is very useful for many applications such as multi-channel systems, and frequency synthesizers.

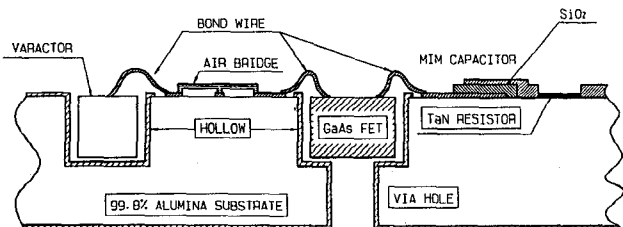


Fig.6 Cross section of the semi-monolithic vco

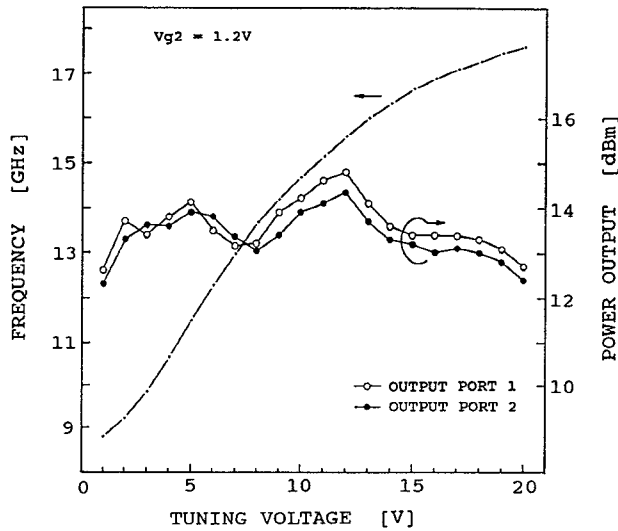


Fig. 7 Measured tuning bandwidth and output power of the VCO

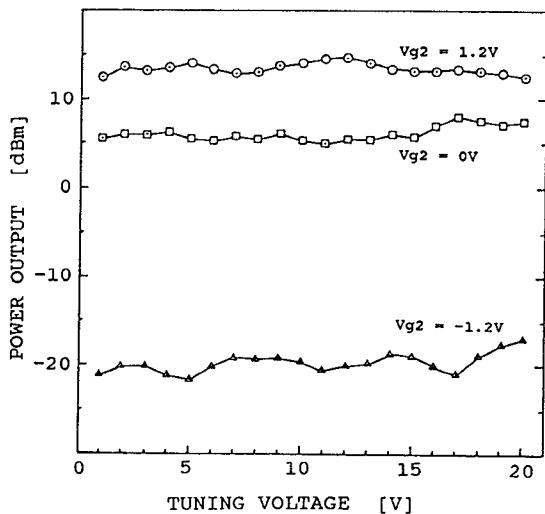


Fig. 8 Measured output power as a function of the second gate voltage

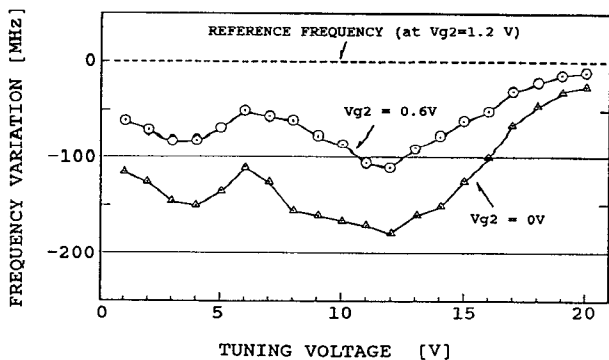


Fig. 9 Frequency variation as a function of the second gate voltage

Table 1. Performance

| | |
|--|----------------|
| FREQUENCY | 8.8 - 17.6 GHz |
| OUTPUT POWER PORT 1 | 13.6 ± 1.2 dB |
| PORT 2 | 13.4 ± 1.2 dB |
| OUTPUT POWER CONTROL VARIATION | > 30 dB |
| OUTPUT POWER MATCH BETWEEN PORT 1 AND PORT 2 | < 0.6 dB |
| FREQUENCY VARIATION VS Vg2=1.2 TO 0 V | < 180 MHz |
| FREQUENCY PULLING (1.7:1 VSWR) | < 50 MHz |
| PHASE NOISE (100KHz OFF-CARRIER) | < -70 dBc/Hz |
| CURRENT | 4.0 V, 85 mA |

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